> transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

Kawashima appears to describe a sense amplifier in figure 7 comprising a pair of cross coupled inverters. The inverters each appear to include a pair of transistors of a second conductivity type (68, 75 and 69, 74). The pair of transistors of a second conductivity type also appear to be coupled at a drain region and a source region.

In contrast, Applicants' independent claims 1, 4, 10, 29, 32, 33, 37, 44, and 45 as amended each claim a dual-gate transistor of a second conductivity type. Dependent claims 2-3, 5, 11-12, 34-36, and 38-39 have also been amended to include a dual-gate transistor for agreement of terms with these independent claims. Nowhere does Kawashima include, teach or suggest the use of a dual-gate transistor in a sense amplifier.

Because Kawashima does not include within its corners all elements of Applicants invention, a 35 U.S.C. §102(b) rejection is no longer appropriate. Applicants respectfully contend that the independent claims as amended and all claims depending therefrom are in condition for allowance. Therefore, Applicants respectfully request withdrawal of Examiner's §102(b) rejection as to claims 1-16, 29-39, 44, and 45.

Rejection under 35 U.S.C. §102(e)

Claims 1-16, 29-39, 44 and 45 were rejected under 35 U.S.C. §102(e) as being anticipated by Austin (US Patent No. 5,982,690). Applicants do not admit that the Austin patent is prior art to the present invention and reserve the right to swear behind this patent at a later date. Applicants also believe that the Austin patent is distinguishable from the present invention. Examiner's rejection states:

> Austin describes in figure 1D a sense amplifier (105) comprising: a pair of cross-coupled inverters (153, 155 and 154, 156), wherein each inverter includes: a transistor of a first conductivity type (P5, P6), a pair of transistors of a second conductivity type (N5, N6, N7, N8) coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type; a pair of bit lines (output of 103), wherein each one of the pair of bit lines is coupled to a gate of a first one of the pair of transistors in each inverter; and a pair of output transmission lines (lat, /lat), wherein each one of the pair of output transmission

lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

Austin appears to describe a sense amplifier 105 comprising a pair of cross coupled inverters. The inverters each appear to include a pair of transistors of a second conductivity type (N5, N6 and N7, N8). The pair of transistors of a second conductivity type also appear to be coupled at a drain region and a source region.

In contrast, Applicants' independent claims 1, 4, 10, 29, 32, 33, 37, 44, and 45 as amended each claim a dual-gate transistor of a second conductivity type. Dependent claims 2-3, 5, 11-12, 34-36, and 38-39 have also been amended to include a dual-gate transistor for agreement of terms with these independent claims. Nowhere does Austin include, teach or suggest the use of a dual-gate transistor in a sense amplifier.

Because Austin does not include within its corners all elements of Applicants invention, a 35 U.S.C. §102(e) rejection is no longer appropriate. Applicants respectfully contend that the independent claims as amended and all claims depending therefrom are in condition for allowance. Therefore, Applicants respectfully request withdrawal of Examiner's §102(e) rejection as to claims 1-16, 29-39, 44, and 45.

Rejection under 35 U.S.C. §103 over Austin

Claims 8, 9, 15-22, 30 and 31 were rejected under 35 U.S.C. §103(a) as being unpatentable over Austin (US Patent No. 5982690). Applicants respectfully maintain their right to swear behind the Austin reference as discussed above.

As to claims 8, 9, 15, 16, 30, and 31 the Examiner's rejection states that "Austin's figure 1D shows all elements of the claimed invention except that it does not show the value of the supply voltage is less than 1.0 Volts and the output delay times is less than 10 ns." As to claims 17-22, Examiner's rejection also states that "Austin's figure 1D shows all elements of the claimed invention except that it does not show the dual-gated MOSFET transistors included in the first and second inverters. However, it would have been obvious to one having ordinary skill in the art to replace the pairs of transistors (153 and 154) with the dual-gated MOSFET transistors for the purpose of saving space."

Applicants respectfully contend that Austin taken alone or in combination with general knowledge in the art does not show all elements of the claimed invention as amended. Independent claims 4, 10, 17, and 29 upon which the cited claims depend all either claim or have been amended to claim a dual-gate transistor.

Austin alone does not show all elements of the claimed invention. The Examiner has stated that Austin contains a pair of transistors of second conductivity type (N5, N6, N7, N8) but, as further cited by the Examiner, Austin "does not show a dual-gated MOSFET" in the sense amplifier 105.

Applicant traverses Examiner's assertion from Examiner's paragraph 6 that "it would have been obvious to one having ordinary skill in the art to replace the pairs of transistors (153 and 154) with the dual-gate MOSFET transistors" and respectfully requests a reference, pursuant to M.P.E.P. Section 2144.03, which describes the use of dual-gate transistors in a sense amplifier in order to support the Examiner's position.

Applicants do not admit that the dependent elements of a supply voltage less that 1.0 volts or an output delay time of less than 10 ns are in the general knowledge of the art. Nonetheless, if the element of a supply voltage less than 1.0 volts is added to Austin, the reference still does not contain, suggest or teach the use of a dual-gate transistor in a sense amplifier. Likewise if the element of an output delay time less than 10 ns is added to Austin, the reference still does not contain, suggest or teach the use of a dual-gate transistor in a sense amplifier.

Therefore, with regard to claims 8, 9, 15-22, 30, and 31, Austin neither independently, nor combined with the added elements of: a supply voltage less than 1.0 Volts; and an output delay time less than 10 ns, contains each and every element of Applicants' claimed invention. Accordingly, withdrawal of Examiner's 35 U.S.C. §103(a) rejections with respect to these claims is respectfully requested.

Rejection under 35 U.S.C. §103 over Kaneko in view of Austin

Claims 23-28 and 40-43 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kaneko et al. (US Patent No. 6069828) in view of Austin (US Patent No. 5982690). Applicants respectfully maintain their right to swear behind the Austin reference as discussed

above. Applicants contend that Austin and Kaneko taken either independently or in combination do not contain, teach, or suggest all elements of Applicants' claimed invention.

With regard to Applicants' independent claims 23 and 40, Austin appears to describe a pair of transistors of second conductivity type (N5, N6, N7, N8) as used in a sense amplifier 105 as shown in Austin's figure 7. Austin does not, however, show a dual-gate transistor as recited in amended independent claims 23 and 40 of Applicants' invention. As cited by the Examiner, the Austin reference taken alone "does not show the dual-gated MOSFET transistors included in the first and second inverters."

Further, Kaneko appears to describe a memory circuit that includes a number of memory arrays (two sides of sense amplifier 15); a sense amplifier (15) and a complementary pair of bit lines (BL1, /BL1, BL2, /BL2) input to the sense amplifier. Kaneko, as noted by the Examiner, "does not show the sense amplifier comprising a pair of cross coupled inverters, wherein each inverter includes a pair of parallel n-channel transistors coupled in series with a p-channel transistor." Neither does is contain, teach or suggest a dual-gate transistor as recited in amended claims 23 and 40 of Applicants' invention. Thus Kaneko does not cure the deficiencies of Austin with the necessary dual-gate transistor element.

Because the references Austin and Kaneko taken independently or in combination do not contain, teach or suggest a dual gate transistor, the cited references do not contain each and every element of Applicants' claimed invention as amended. Applicants therefore respectfully contend that independent claims 23 and 40 as amended are not obvious over Kaneko in view of Austin. Applicants respectfully request that Examiner's §103(a) rejections be withdrawn with respect to independent claims 23 and 40, and also their dependent claims 24-28 and 41-43 as depending on allowable claims.

CONCLUSION

Applicants respectfully submit that the claims 1-45 as amended are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6913 to facilitate prosecution of this application.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 9/21/2000 By _____
Edward J. Brooks, III
Reg. No. 40,925

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents, Washington, D.C. 20231 on **August 21, 2000**.

Tina Pugh
Name

_____
Signature